Transmission-Line Load-Network Topology for Class-E Power Amplifiers

Andrew J. Wilkinson, *Member, IEEE*, and Jeremy K. A. Everard, *Member, IEEE*

***Abstract*—Class-E amplifiers are a type of switching amplifier offering very high efficiency approaching 100% . In this paper, a topology and design methodology, which could be used for a transmission-line implementation of a class-E power amplifier, is presented. A simple transmission-line class-E load network is proposed that offers combined transformation of the load resistance down to a suitable level, as well as simultaneous suppression of harmonics in the load. The load network was developed and tested with the aid of a time-domain simulator (i.e., SPICE). A microstrip layout was designed and a first prototype was built operating at 1 GHz utilizing a field-effect transistor as the switching device. A drain efficiency of 72% was measured for our prototype after tuning, although better performance can be expected with an improved switching transistor and careful tuning of the load network.**

***Index Terms*—Amplifier, class E, high efficiency, microstrip, power, transmission line.**

I. Introduction

CLASS-E switching amplifiers offer high-efficiency conversion of dc to ac via careful design of the transient waveforms of a resonant load network. The concept was first proposed by Sokal and Sokal [1] and design equations for an idealized topology were derived by Raab [2], [3]. High efficiency approaching 100% is achieved by tailoring the transient response of the voltage and current waveforms to minimized energy loss at the switching instants.

Earlier class-E designs have concentrated on the development of lumped-element load-network topologies for RF applications operating in the megahertz range; both narrow-band [1], [4] and broad-band networks [5], [6] have been developed. In the microwave region, lumped elements are not so easily fabricated and may depart from idealized components. To address this problem, we proposed, developed, and tested [7] a transmission-line class-E load network that we envisaged would find application in the construction of microwave power amplifiers. In this paper, we describe in detail the transmission-line topology, design methodology, simulated waveforms, and performance, as well as the implementation and performance of the distributed microstrip prototype operating at 1 GHz.[1]

Manuscript received February 1, 2000; revised December 1, 2000. This work was supported by the U.K. Engineering and Physical Sciences Research Council.

A. J. Wilkinson is with the Department of Electrical Engineering, University of Cape Town, Rondebosch 7701, Cape Town, South Africa.

J. K. A. Everard is with the Department of Electronics, University of York, Heslington, York YO10 5DD, U.K.

Publisher Item Identifier S 0018-9480(01)04442-8.

[1]This paper reports on work undertaken in 1991 while the authors were at Kings College London, London, U.K.

Recent developments in the literature include a transmission-line circuit utilizing a series line and single shunt stub to achieve class-E operation [8], and a power-combining four-transistor class-E amplifier [9] employing GaAS MESFETs to obtain an output power 2.95 W at 935 MHz, with a power-added efficiency of 67%.

This paper is organized as follows. Section II reviews the principles behind the class-E concept. Section III describes the proposed transmission-line topology and simulated time-domain waveforms. Section IV describes the design, implementation, and performance of a microstrip prototype. Section V describes a second transmission-line topology in which the dc choke is replaced by a short inductive transmission-line section. Conclusions are then given in Section VI.

II. Class-E Amplifiers

Switching amplifiers are amplifiers for which the active device (or devices) approximates the operation of an idealized switch exhibiting a high impedance in the "off" state and a low impedance in the "on" state. In the ideal case of zero "on" resistance and infinite "off" resistance, no power is dissipated in the switching device, except at the switching instants. In practical transistor circuits operating at high RF frequencies, a significant cause of energy loss is the short circuiting of the energy stored in the parasitic capacitance $((1/2)CV^2)$ across the transistor as the switch closes. A lesser effect is the relatively small amount of energy stored in the parasitic series inductance of the device $((1/2)L_sI_s^2)$, which is lost as the switch opens. Other sources of loss include a nonzero "on" resistance and a noninfinite "off" resistance.

The class-E switching amplifier concept [1] aims to achieve high efficiency by designing the voltage and current waveforms so as to minimize losses at the switching instants. As described in [1], the ideal operation requires that the voltage V_s across the device drops to zero immediately before the switch closes, and the current I_s through the device drops to zero immediately before the switch opens.

A. Simple Lumped-Element Topology

An example of a simple class-E switching amplifier is shown in Fig. 1(a). The switching device is assumed to contain a parasitic shunt capacitance C_1 and negligible series inductance. The load network forms a series resonant circuit for which the components can be chosen such that transient waveforms achieve idealized class-E operation.

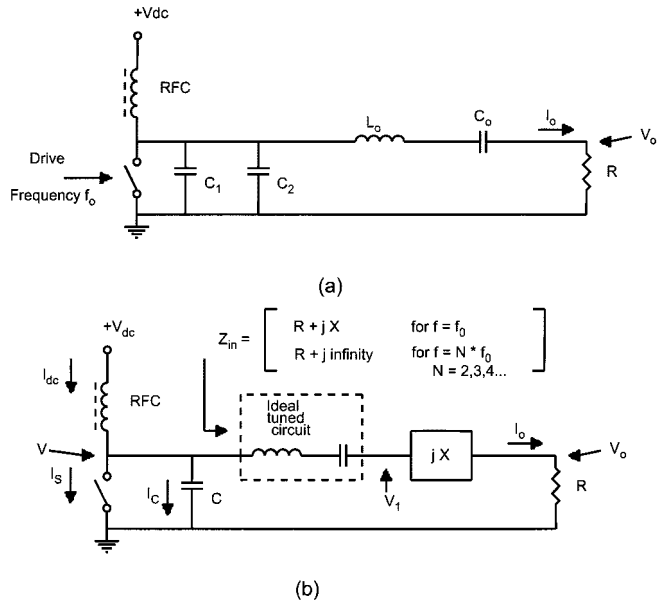


Fig. 1. (a) Lumped-element class-E amplifier. (b) Equivalent circuit.

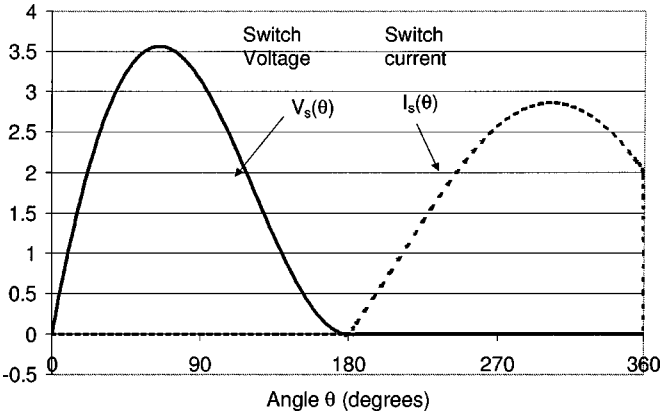


Fig. 2. Class-E switch waveforms.

B. Idealized Operation

The circuit shown in Fig. 1(a) was analyzed in detail by Raab [2] who derived analytical expressions for the idealized equivalent circuit depicted in Fig. 1(b). His analysis assumes (1) power is fed to the circuit via a RF choke of infinite inductance (current $I_{\rm dc}$ is constant) (2) the output filter passes only the fundamental f_0 to the load resistor and presents an infinite impedance at all harmonics. Parasitic capacitance C_1 is lumped together with the additional capacitor C_2 in capacitor C.

The waveforms for the case of a 50% switching duty cycle are shown in Fig. 2. The voltage across the switch drops to zero at the switch-on instant and also is designed to have zero slope, hence, relaxing the switch speed requirement.

In the following section, the main results of the analysis given by Raab are summarized for their relevance to the explanation of the transmission-line topology in subsequent sections.

C. Class-E Design Equations

Reproduced below are the design equations [2] for an idealized class-E amplifier with a 50% duty cycle and zero voltage and zero derivative at the switch-on instant. Component symbols are depicted in Fig. 1(b).

$$\text{Output power:}\quad P_o = \frac{V_{\rm dc}^2}{R_{\rm dc}} \tag{1}$$

$$\text{Equivalent dc resistance:}\quad R_{\rm dc} = 1.7337R \tag{2}$$

$$\text{Shunt susceptance:}\quad B = wC = \frac{1}{5.4466R} \tag{3}$$

$$\text{Load angle:}\quad \psi = 49.052^\circ \text{ (inductive)} \tag{4}$$

$$\text{Load-network impedance:}\quad Z = R + jX \tag{5}$$

$$\text{where:}\quad X = R\tan\psi = 1.152R \tag{6}$$

$$\text{Peak switch voltage:}\quad V_{s\max} = 3.56V_{\rm dc} \tag{7}$$

$$\text{Peak switch current:}\quad i_{s\max} = 2.84I_{\rm dc}. \tag{8}$$

For a given specified output power P_o and supply voltage $V_{\rm dc}$, the required switch capacitance C and load reactance $R + jX$ may be calculated. The idealized waveforms for the case $V_{\rm dc} = 1$ and $P_o = 1$ are shown in Fig. 2.

Raab's equations can be used to design a practical class-E amplifier based on the narrow-band high-Q topology shown in Fig. 1(a).

III. Transmission-Line Topology

This section describes the design and development of the proposed transmission-line topology (in more detail than first reported in [7]).

A. Design Objectives

Our primary aim was to develop a narrow-band load network consisting of only distributed transmission-line elements. In our first design, this requirement was relaxed to allow the presence of an ideal RF choke as the dc feed (in Section V, a topology is discussed which replaces the choke with a transmission line); additionally, it was assumed that a lumped capacitor (of negligible reactance) could be present to block any dc component from reaching the load resistor. The load network should exhibit the following desirable properties.

- The load network should present a high reactive impedance at harmonics of the fundamental.
- The network should suppress all harmonics to a low level at the load (e.g., better than 40 dB below the fundamental).
- The load resistance (typically 50 Ω) should be appropriately transformed down to a practical value to achieve the required output power. This should also take into account the "on" resistance of the active switch and the current through and voltage across the active device.
- The peak voltage across the switch and peak current through the switch should not exceed device specifications.
- The topology should be easily converted to a microstrip realization, and should be as "simple" as possible.

B. Design Methodology

The approach taken in the development of the transmission-line load-network topology was as follows.

1) A realistic specification for a transistor amplifier design was first considered and typical ballpark values were calculated for the load-network input resistance R taking into account load resistance, required output power, and limits of the transistor breakdown voltage and current.
2) A lumped-element circuit was then designed that would satisfy the specifications and also provide adequate suppression of harmonics to the load.
3) The lumped circuit was then converted to an equivalent transmission-line circuit, carefully observing the impedances of the transmission-line elements at higher harmonics.
4) The circuit was then simulated to validate its operation and components were tuned to obtain ideal class-E waveforms.
5) The transmission-line design was then converted to a distributed microstrip layout.
6) A prototype circuit was built and tested.

1) Design Considerations: As a starting point, we considered the goal of designing a 1-GHz class-E amplifier delivering 1 W into a 50-Ω resistive load. It was assumed an FET would be used as the active switch, with an "on" resistance of around 1 Ω and a capacitance of around 2 pF. The efficiency of the practical class-E amplifier is limited by the "on" resistance of the device implying that a high load-network resistance R is required. On the other hand, a high value of R implies a large supply voltage to achieve the desired output power [as dictated by (1) and (2)]. Assuming an FET breakdown voltage of, say, 15 V, the maximum supply voltage would be limited to $15/3.56 = 4.2$ V [from (7)]. In terms of the output power P_o and maximum switch voltage $V_{s\max}$, the resistive component of the impedance of the load network is given [from (1), (2) and (7)] by

$$R = \frac{R_{\rm dc}}{1.7337} = \frac{V_{\rm dc}^2}{1.7337 P_o} = \frac{(V_{s\max}/3.56)^2}{1.7337}.$$

To achieve a power output of 1 W, a value of $R \approx 10\ \Omega$ is required. The inductive reactance $X = 11.5$ is chosen providing a load angle $\psi = 49.0°$.

The required switch shunt capacitance according to (3) is $C = 1/(5.4466\, R\omega) = 2.92$ pF.

2) Initial Lumped-Element Topology: From practical considerations, it was concluded that a step down stage would be required for driving a 50-Ω load. To achieve the required transformation, as well as to provide satisfactory suppression of harmonics in the load, a two-stage cascaded low-pass L-type transformer was proposed. The circuit topology is shown in Fig. 3—actual component values are shown for an impedance transformation from 50 Ω down to 10 Ω at the reference plane. The first L-piece (3.54 pF and 3.96 nH) transforms from 50 Ω down to 22 Ω and the second stage (7.91 pF and 1.77 nH) transforms from 22 to 10 Ω. The additional inductive phase angle is provided by adding additional series inductance.

3) Conversion of the Lumped-Element Circuit to a Transmission-Line Equivalent: The conversion of the lumped-element circuit involved replacing the series inductances and shunt capacitances with equivalent transmission-line elements. The series inductances can be realized by short sections (less than $\lambda/8$) of a high-impedance line [10], and shunt capacitors by lower impedance open-circuit stubs.[2]

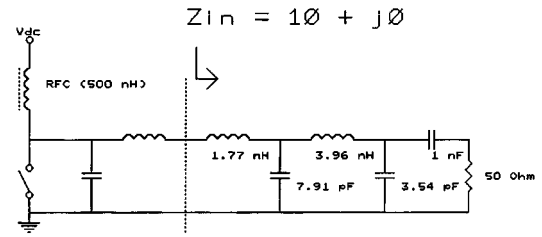


Fig. 3. Lumped-element model with impedance transformation stages.

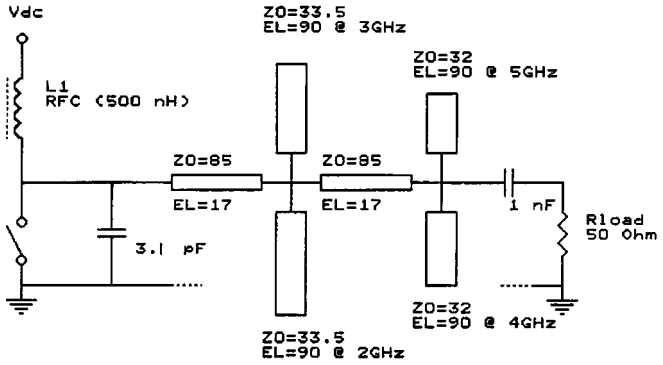


Fig. 4. Transmission-line topology (operating at 1 GHz).

The electrical parameters of the capacitive stubs can be engineered to provide simultaneously the correct reactance at the fundamental frequency f_0 (for the impedance transformer), as well as provide enhanced suppression of harmonics reaching the load by arranging the stub lengths to have low input impedance at selected harmonics (i.e., short circuiting the harmonic to ground). This is achieved by choosing the stub length such that its electrical length is exactly 90° at the particular harmonic that one would like to suppress. The impedance of the stub is then chosen to provide the desired capacitive reactance at the fundamental. Fig. 4 shows our proposed transmission-line topology (for the 1-GHz design example). Each shunt capacitor has been replaced by two stubs, providing for harmonic suppression at four frequencies. The stubs were chosen to have an electrical length of 90° at frequencies $2f_0$, $3f_0$, $4f_0$, and $5f_0$. It is noted that the input impedance of a stub, which is a quarter-wavelength long at frequency f_x, will also have a low impedance at frequencies $f_x(1+2k)$, where k is a positive integer, i.e., at frequencies $\{3f_x, 5f_x, 7f_x, \ldots\}$, assuming the propagation velocity is frequency independent. Table I lists the first three frequencies suppressed by each of the four harmonic stubs.

As can be seen in Table I, if four stubs that are a quarter-wavelength at each of the first four harmonics are used, suppression at the fifth, eighth, ninth, and other higher harmonics will also be achieved. The harmonic content of the switch voltage decays with increasing frequency, and it was found via simulation that actively suppressing the first five appeared suffi-

[2]The equivalent inductance of a short transmission-line section is $L = (Z_0\, EL)/(f\, 360)$, where Z_0 is the characteristic impedance, f is the frequency, and EL is the electrical length in degrees [10]. The equivalent capacitance of a short open-circuit stub is $C = (EL)/(Z_0\, f\, 360)$.

TABLE I
FIRST THREE FREQUENCIES SUPPRESSED BY EACH OF THE FOUR HARMONIC STUBS

1^{st} harmonic stub:	$2f_0$	$6f_0$	$10f_0$
2^{nd} harmonic stub:	$3f_0$	$9f_0$	$15f_0$
3^{rd} harmonic stub:	$4f_0$	$12f_0$	$20f_0$
4^{th} harmonic stub:	$5f_0$	$15f_0$	$25f_0$

cient to keep all higher harmonics over 40 dB below the fundamental. In practice, additional suppression of other higher harmonics (e.g., sixth and seventh) can easily be achieved by including additional harmonic stubs in the design. It is noted that the short-circuit harmonic stub topology also makes the network's input impedance *at the harmonics* independent of the impedance of the actual "50-Ω" load. This could be advantageous when driving a load such as an antenna, which may only be properly matched to 50 Ω at the fundamental.

4) Time-Domain Simulation and Tuning: In order to investigate the performance of the load network, the EESOF suite of simulation and modeling tools was used. The load network was programmed into the TOUCHSTONE simulator and plots were obtained of the frequency response of the network from dc to 11 GHz. The impedance looking into the L-type impedance transformer was trimmed to match that of the lumped-element topology (this was done by starting at the load end and adding components down the chain, trimming the characteristic impedance of the capacitive stubs to achieve the same impedance as the lumped model, and similarly trimming the electrical length of the inductive pieces). The input impedance was accurately adjusted to $10 + j0\ \Omega$. An additional high impedance length was then added to the input transmission line to modify the load angle to 49° inductive (excluding the switch capacitor), as required for idealized class-E operation. It is noted that Raab's analysis assumes infinite load impedance at the harmonics. For our network, this is not quite true and, thus, some tuning of the load network would be required to achieve zero switching voltage and slope.

To check the harmonic suppression of the load network, the S-parameter S_{21} response was plotted over the 1–11-GHz range. Fig. 5 shows that deep nulls occur at the first five harmonics.

In order to verify the operation, SPICE was used to simulate the transient behavior of the load network. The switch was modeled as idealized switch with an "on" resistance of 1 Ω and a shunt capacitance of 2.92 pF. The dc supply voltage was set to 3.5 V, implying an output power (for an ideal switch) of $P_o = V_{\text{dc}}^2/(1.7337R) = 0.71$ W. After allowing the waveforms to reach near steady state (about 200 cycles), the collector voltage was monitored at the switching moment. It was found that typical class-E behavior did occur, although some tuning of the shunt capacitance and load angle was required to achieve zero voltage and slope at the switching instant. It was found that satisfactory operation could be achieved by increasing the switch capacitance to 3.1 pF and also extending the electrical length of the inductive line at the network input (the load angle at the fundamental was increased to $\psi = 55.8°$). Plots of the tuned load network's input impedance and magnitude can be seen in Figs. 6 and 7. The switch voltage and current waveforms and switch capacitor current obtained (after tuning) are shown in Fig. 8, as well as the voltage across the load resistor.

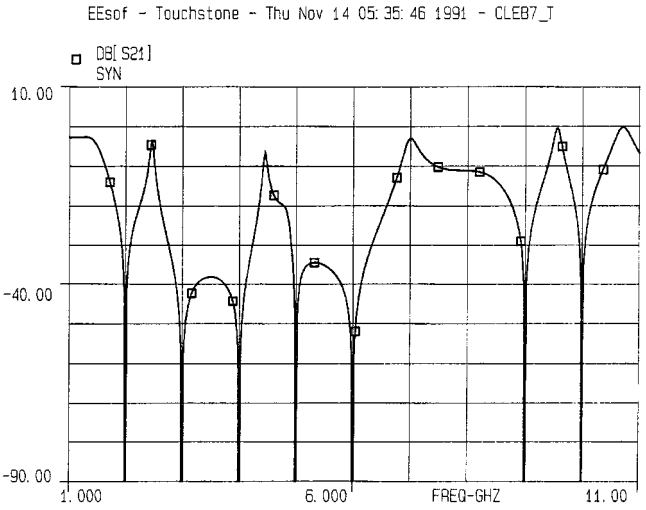


Fig. 5. Simulated S_{21} response of transmission-line load network (1–11 GHz).

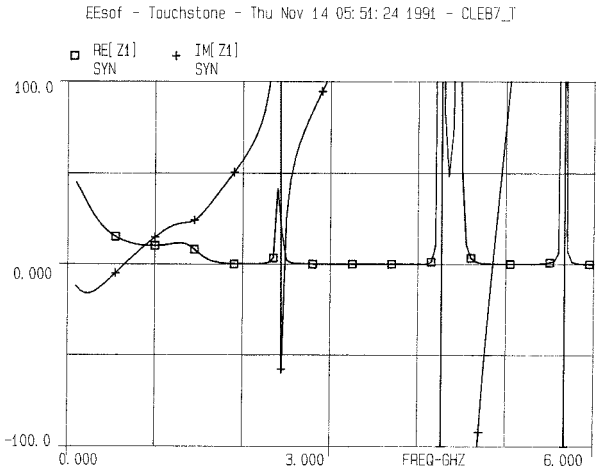


Fig. 6. Real and imaginary components (calculated) of the impedance at the input of the transmission-line load network (0–6 GHz).

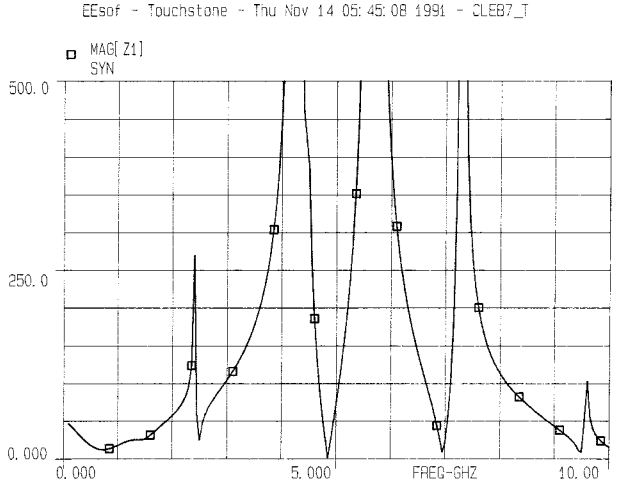


Fig. 7. Magnitude (calculated) of the input impedance of the transmission-line load network.

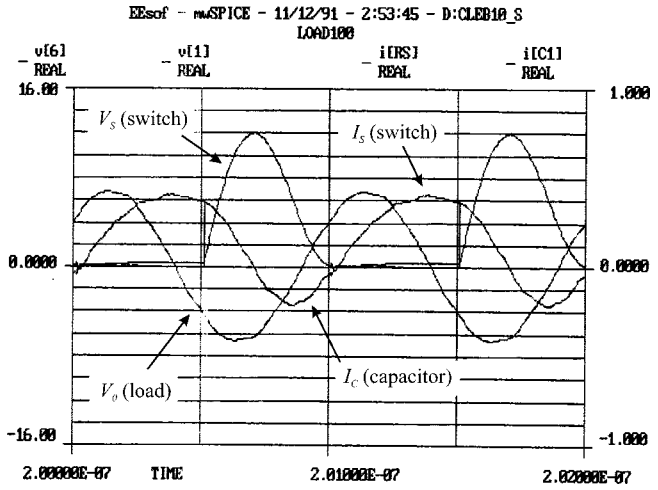


Fig. 8. Simulated waveforms: $f = 1.0$ GHz.

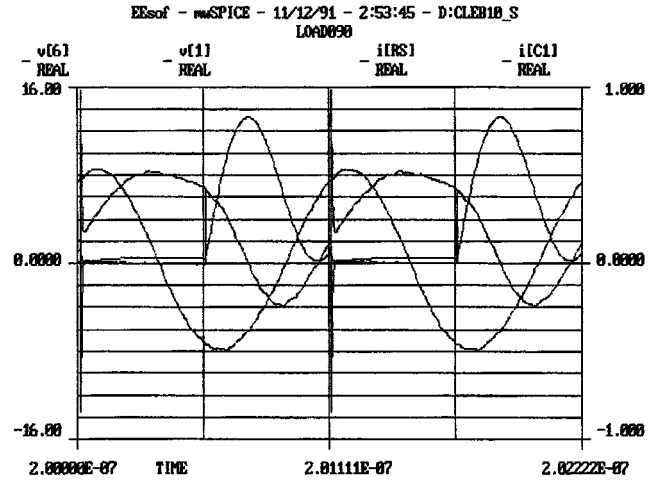


Fig. 9. Simulated waveforms: $f = 0.9$ GHz.

The finite 1 Ω "on" resistance results in a small voltage rise (see waveform) during the "on" part of the cycle.

One of our concerns was the degree of accuracy of the SPICE simulations—we tried to ensure trustworthy results by reducing the simulator time step to 0.001 ns and allowing sufficient time to reach steady state. We also checked that the dc input power $V_{\rm dc}I_{\rm dc}$ balanced the power dissipated in the circuit. One check we did involved setting the switch resistance to a negligibly low value of 0.001 Ω (setting it to zero caused numerical problems), retuning for zero switch voltage at switch on, and then comparing the ratio of the power in the load to the dc input power—an accurate simulation should yield a ratio (or efficiency) close to one—after reducing the step size and allowing the circuit to reach "steady state," the ratio reached 0.96. The same simulator parameters were then applied to the case of an "on" resistance of 1 Ω and tuning was performed as described.

The circuit behavior with drive frequencies of 0.8, 0.9, 1.1, and 1.2 GHz was also simulated. The time-domain waveforms at 0.9 and 1.1 GHz are shown in Figs. 9 and 10. Plots of the power output, efficiency, and first harmonic level below fundamental

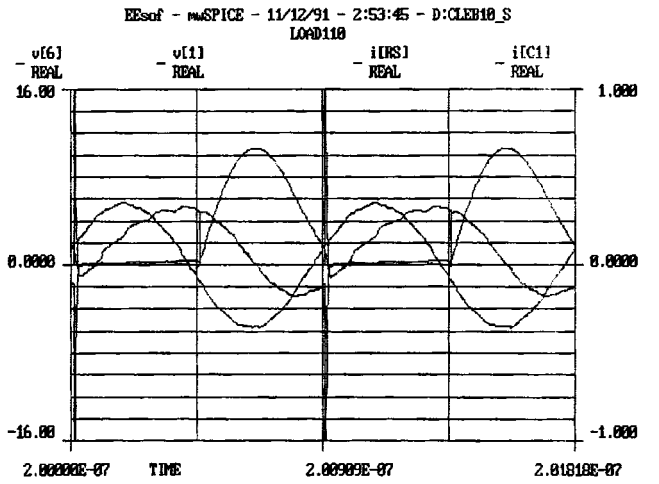


Fig. 10. Simulated waveforms: $f = 1.1$ GHz.

as a function of drive frequency are shown in Fig. 11(a)–(c). The simulated efficiency at 1 GHz was 90%.

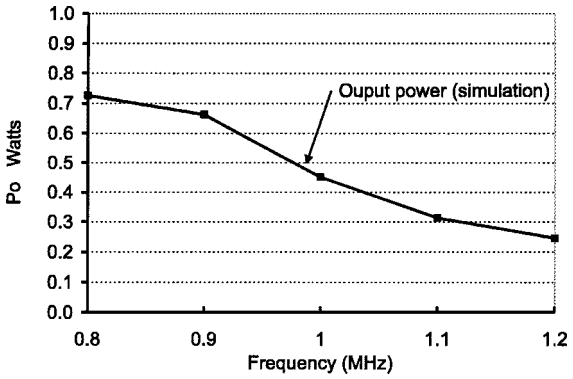
5) Microstrip Realization of Load Network: Having obtained promising results with the simulation, the load network was converted to an equivalent microstrip implementation. The printed circuit board (PCB) used was a low-loss RT Duroid RT5880, which has a relative dielectric constant of 2.2, a loss tangent of 0.009 at 10 GHz, a dielectric thickness of 0.381 mm, and a copper thickness of 0.034 mm. The microstrip layout of the load network is shown in Fig. 12. The series inductance sections in Fig. 12 were implemented with 85-Ω sections (width ∼0.44 mm, wavelength $\lambda_g \sim 224$ mm at 1 GHz). The capacitive stubs were implemented with broader 32-Ω sections (width ∼2.14 mm, $\lambda_g \sim 214.5$ mm at 1 GHz) and 33.5-Ω sections (width ∼2.01 mm, $\lambda_g \sim 214.9$ mm at 1 GHz). The transmission-line loss was considered negligibly small; e.g., a 5-cm length of an 85-Ω line has a loss of 0.09 dB or a fractional power reduction of 2% for a forward-traveling wave at 1 GHz.

With the aid of the TOUCHSTONE simulator, the physical lengths of the stubs were adjusted to have the correct electrical lengths of 90° at the corresponding stub frequencies $2f_0$, $3f_0$, $4f_0$, and $5f_0$. Plots of the frequency response of the TOUCHSTONE microstrip model closely approximated the ideal transmission-line frequency response.

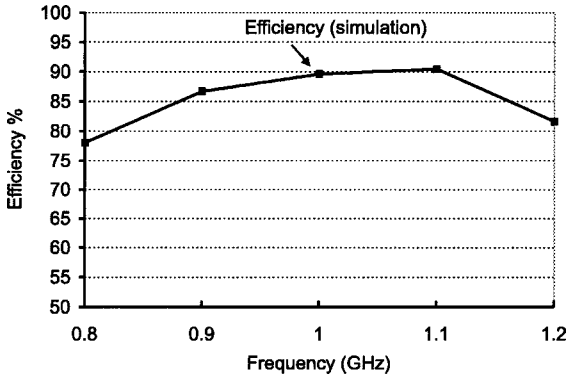
A PCB was etched with the class-E load network and the input impedance and transmission loss (S_{21}) were measured from 1 up to 11 GHz with an HP network analyzer. The response (Fig. 13) closely matched the desired response (compared to Fig. 5) with deep nulls at the first five harmonics.

IV. Experimental Prototyping

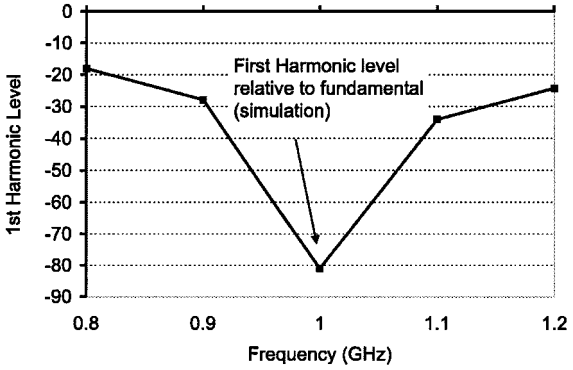
In order to test the proposed transmission-line topology, a microstrip amplifier operating at 1 GHz was constructed. For comparison purposes, a lumped-element amplifier was first constructed and tested using the same active device used in the microstrip design. The active device was a readily available Avantek ATF 8140 GaAs FET, the parameters of which are summarized in Table II.



(a)



(b)



(c)

Fig. 11. Simulated: (a) output power, (b) efficiency, and (c) first harmonic level.

A. Prototype Lumped Amplifier At 900 MHz

Before building the microstrip implementation, some experimenting was done with a lumped-element prototype (using the ATF 8140 FET). The circuit is shown in Fig. 14. As with the 1-GHz microstrip design, the 50-Ω load was transformed down to 10 Ω—although in the lumped circuit, this was done with a single-stage L-type transformer. The load network has a loaded Q of about five. The input impedance to the load network was checked and tuned with a network analyzer to the desired value. The amplifier was then operated with sufficient input drive to "switch" the FET, and tuned for maximum drain efficiency (this involved trimming both the 1.2-pF switch capacitance and the load-angle 4.8-pF capacitance). The results are summarized in Table III.

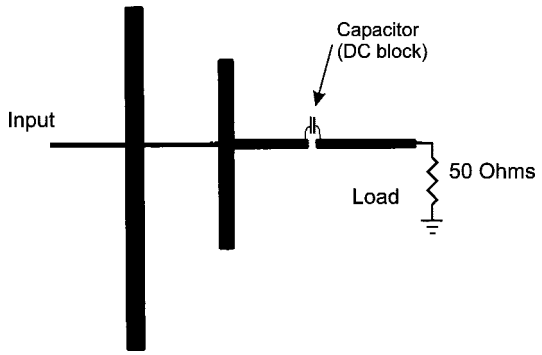


Fig. 12. Microstrip realization of load network (scale not 1 : 1).

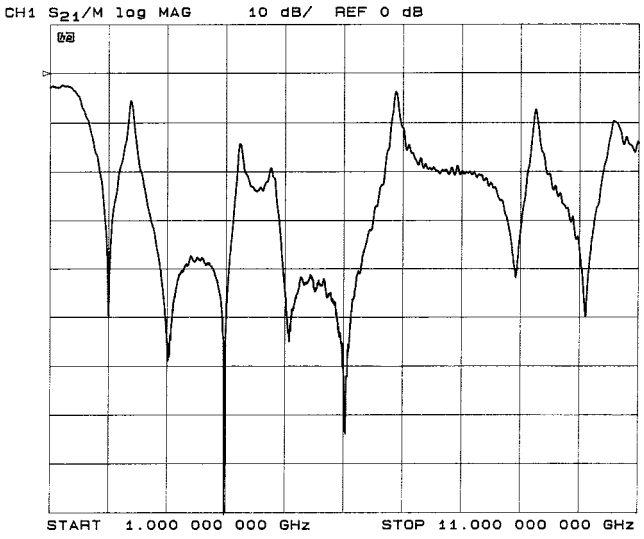


Fig. 13. Measured S_{21} response of actual microstrip load network (1–11 GHz).

TABLE II
AVANTEK ATF 8140 GaAs FET PARAMETERS

Breakdown voltage (data sheet)	15 Volts
DC "on" resistance (measured)	0.8 Ohms
Drain-Source Capacitance	2.5 pF
Gate Voltage for "off state"	-6 Volts
Gate Voltage for "on state"	0 Volts
Input impedance ($Vg = -4V$) at 1GHz	$4.5 - j16\ \Omega$

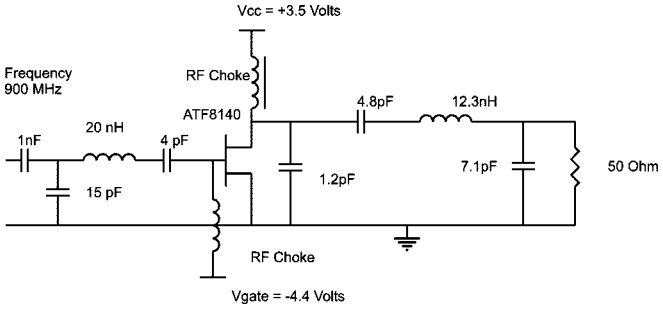


Fig. 14. Experimental 900-MHz lumped-element class-E amplifier.

A maximum drain efficiency of 72% was achieved at 900 MHz. It was found that the efficiency was sensitive to supply voltage—increasing the supply voltage to 4.0 V and dropped the drain efficiency to 60% . These figures were

TABLE III
MEASURED PERFORMANCE OF THE 900-MHz LUMPED-ELEMENT AMPLIFIER—AFTER TUNING

DC Supply Voltage	3.5 Volts
DC current	0.182 Amps
DC input power	0.637 Watts
AC output power	0.457 Watts
Drain efficiency	72 %

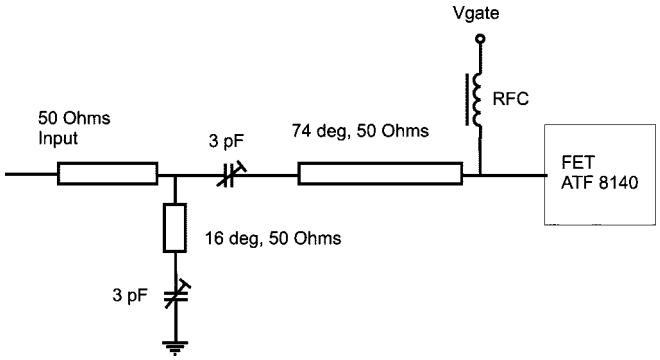


Fig. 15. Tunable matching circuit.

somewhat disappointing, as it had been hoped to achieve efficiencies approaching the simulated value of around 90%. The difference may be due to a number of possible causes. In our simulation, the switch was modeled as having a perfect 50% duty cycle, with an "on" resistance of 1 Ω. As it was not possible to observe the waveforms on an oscilloscope, it could not be verified that the FET was, in fact, switching as in our simulation (this suggested that perhaps a faster FET should be acquired for testing the distributed prototype). Another source of loss is radiation from the output network.

The above concerns were not investigated further (mainly owing to time constraints) and it was decided to continue building the distributed microstrip prototype hoping for comparable or better performance.

B. Prototype Distributed Microstrip Amplifier

A prototype microstrip amplifier was constructed on a test jig using the load network in Fig. 4 and corresponding microstrip realization in Fig. 12. An adjustable input matching network was designed to provide a match at the gate "pinchoff" voltage of −4 V. The input matching network is shown in Fig. 15. The microstrip layout for the prototype jig is shown in Fig. 16.

The FET drain–source capacitance was approximately 2.5 pF, which is 0.6 pF less than the required switch capacitance of 3.1 pF. The additional 0.6-pF capacitance of was made up of two short capacitive stubs attached at the point where the FET source connects to the load network (see Fig. 16).

To avoid exceeding the breakdown voltage and possibly destroying the FET, the test circuit was operated with a dc supply voltage of 3.5 V, implying a peak switch voltage of 12.5 V [from (7)], which is below the breakdown voltage of 15 V.

A photograph of the complete amplifier is shown in Fig. 17.

Without any tuning of the output network, a drain efficiency of 59% was measured at 1 GHz. The parameters are given in Table IV.

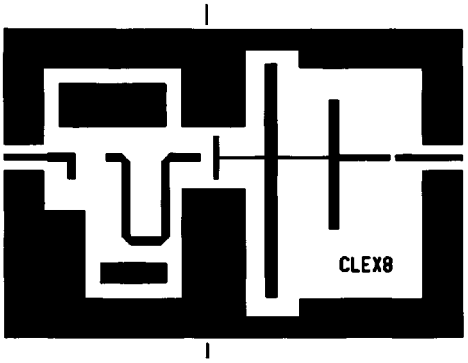


Fig. 16. Microstrip circuit layout, showing the input matching network on the left-hand side and the load network on the right-hand side.

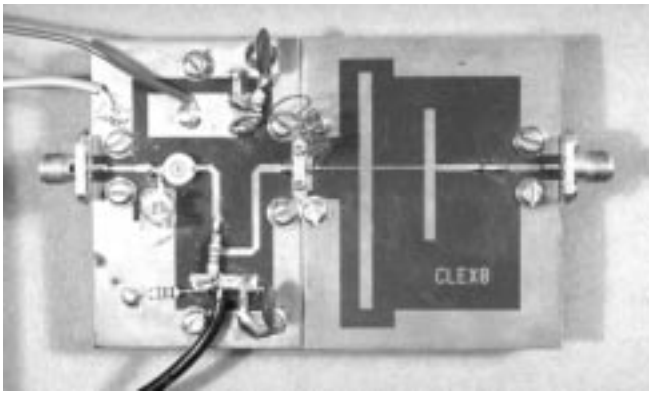


Fig. 17. Prototype microstrip class-E amplifier.

TABLE IV
MEASURED PERFORMANCE OF THE MICROSTRIP AMPLIFIER AT 1.0 GHz—BEFORE TUNING

DC Supply Voltage	3.5 Volts
DC current	0.171 Amps
DC input power	0.600 Watts
AC output power	0.354 Watts
Drain efficiency	59 %

TABLE V
MEASURED PERFORMANCE OF THE MICROSTRIP AMPLIFIER AT 950 MHz—AFTER TUNING

DC Supply Voltage	3.53 Volts
DC current	0.180 Amps
DC input power	0.635 Watts
AC output power	0.458 Watts
Drain efficiency	72 %

Increasing the "switch" shunt capacitance did not achieve much improvement. It became clear that some mechanism of tuning the circuit (both load angle and switch capacitance) had to be incorporated into the microstrip design. One possibility would be to provide a mechanism for adjusting the length of the first inductive line at the input of the network.

In our experimental testing, we were able to obtain a drain efficiency of 72% by reducing the drive frequency to 950 MHz and by simultaneously bending the supply choke lead closer to the

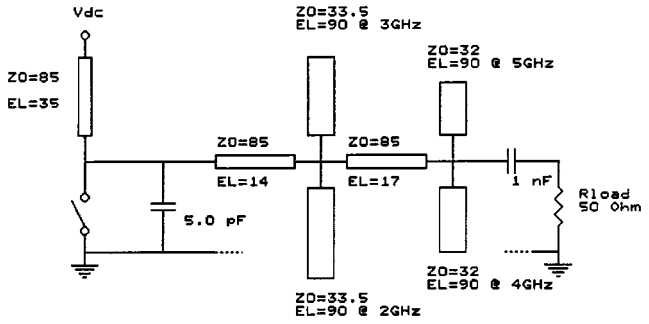


Fig. 18. Transmission-line topology with choke replaced by inductive transmission-line feed.

ground plane. The measured parameters are given in Table V. The results are similar to those obtained with the 900-MHz lumped prototype.

V. Transmission-Line Topology without RF Choke

The transmission-line topology described in Section III used a wire-based RF choke to provide the dc input power. This element can be replaced by a transmission-line section, as shown in Fig. 18. Simulations suggest that, with some adjustment of the switch capacitance, an 85-Ω line with an electrical length of 35° offers similar performance, although care has to be taken in selection of the electrical length to avoid high-frequency resonances. The presence of an inductive element (effectively in parallel with the switch capacitor) could be used to improve (after some optimization) the frequency response, i.e., flatten the output power and efficiency curves over a band. This technique has been successfully applied to the broad-banding of a lumped-element class-E design [5], although we have not investigated this technique in the context of the transmission-line topology.

VI. Conclusions

A simple transmission-line topology for a narrow-band class-E applications has been described. The load network proposed in this paper offers combined transformation of the load resistance down to a suitable level, as well as simultaneous suppression of higher harmonics in the load via the use of stubs of lengths chosen to be a quarter-wavelength at the harmonics.

The class-E operation of the load network has been verified by time-domain simulation indicating that the circuit could be successfully applied in practice.

An experimental microstrip prototype, designed to operate at 1 GHz, was constructed. Experiments indicated that without accurate simulation of the behavior of the active device, tuning is required in practice to optimize efficiency. After some tuning and load-angle adjustment (achieved partly by shifting the drive frequency), a peak drain efficiency of 72% at 0.95 GHz was achieved. It is felt that higher efficiency could be obtained via careful selection of a high-speed FET, and that the circuit behavior and efficiency could be better predicted via simulation if a FET is used for which an accurate large-signal SPICE model is available.

It would of value to build a lower frequency transmission-line version to validate the simulations and design—perhaps operating below 100 MHz using a coaxial cable for the transmission lines. This would have several advantages, including easy visualization of the waveforms, easier tuning of the circuit, and the availability of active devices that closely approximate an ideal switch. We are currently constructing and testing a 10-MHz coaxial line implementation, which we plan to report on in the future.

Further investigation could include replacing the RF choke with a transmission-line section, as proposed in Section V, as well as investigating ways of achieving a flatter frequency response.

References

[1] N. O. Sokal and A. D. Sokal, "Class E—A new class of high-efficiency tuned single-ended switching power amplifiers," *IEEE J. Solid-State Circuits*, vol. SC-10, pp. 168–176, June 1975.

[2] F. H. Raab, "Idealized operation of the class E tuned power amplifier," *IEEE Trans. Circuits Syst.*, vol. CAS-25, pp. 725–735, Dec. 1977.

[3] ——, "Effects of circuit variations on the class E tuned power amplifier," *IEEE J. Solid-State Circuits*, vol. SC-13, pp. 239–247, Apr. 1978.

[4] R. E. Zulinski and J. W. Steadman, "Class E power amplifiers and frequency multipliers with finite DC-feed inductance," *IEEE Trans. Circuits Syst.*, vol. CAS-34, pp. 1074–1087, Sept. 1987.

[5] J. K. A. Everard and A. J. King, "Broadband power efficient class E amplifiers with a nonlinear CAD model of the active MOS device," *J. Inst. Electron. Radio Eng.*, vol. 57, no. 2, Mar./Apr. 1987.

[6] J. K. A. Everard, *Fundamentals of RF Circuit Design with Low Noise Oscillators*. New York: Wiley, 2000, pp. 248–287.

[7] J. K. A. Everard and A. J. Wilkinson, "Highly efficient class E amplifiers," in *IEE Solid-State Power Amp. Colloq. Dig.*, Dec. 16, 1991, pp. 3/1–3/4.

[8] T. Mader and Z. Popović, "The transmission-line high-efficiency class-E amplifier," *IEEE Microwave Guided Wave Lett.*, vol. 5, pp. 290–292, Sept. 1995.

[9] A. L. Martin and A. Mortazawi, "A class-E power amplifier based on an extended resonance technique," *IEEE Trans. Microwave Theory Tech.*, vol. 48, Jan. 2000.

[10] V. F. Fusco, *Microwave Circuits: Analysis and Computer-Aided Design*. Englewood Cliffs, NJ: Prentice-Hall, 1987.

Andrew J. Wilkinson (M'01) was born in Cape Town, South Africa, on March 1, 1968. He received the B.Sc. degree in electrical engineering from the University of Cape Town, Cape Town, South Africa, in 1989, and the Ph.D. degree from the University College London, London, U.K., in 1998.

In 1997, he was a Guest Scientist with the German Aerospace Agency (DLR), where he was involved with radar signal-processing algorithms for synthetic aperture radar interferometry. He returned to Cape Town, South Africa, and joined the Radar Remote Sensing Group, University of Cape Town. In 2000, he became a Senior Lecturer in the Department of Electrical Engineering, University of Cape Town. His research interests include RF and microwave circuits and systems, analog instrumentation, radar signal processing, applications of Bayesian inference, and inverse problems.

Jeremy K. A. Everard (M'90) received the B.Sc. Eng. degree at King's College, University of London, London, U.K., in 1976, and the Ph.D. degree from the University of Cambridge. Cambridge, U.K., in 1983.

He was in industry for six years with the GEC Marconi Research Laboratories, M/A-Com, and Philips Research Laboratories where he worked on radio and microwave circuit design. While with Philips Research Laboratories, he ran the Radio Transmitter Project Group. He then taught RF and microwave circuit design, opto-electronics, and electromagnetism at King's College London, for nine years while leading the Physical Electronics Research Group. In 1990, he became a University of London Reader in Electronics at King's College London and Professor of electronics at the University of York, Heslington, York, U.K., in September 1993. He has authored or co-authored over 60 papers, *Fundamentals of RF Circuit Design with Low Noise Oscillators* (New York: Wiley, 2000), co-edited and co-authored *Gallium Arsenide Technology and Its Impact on Circuits and Systems* (Stevenage, U.K.: Peregrinus, 1989), and contributed to *The Distributed Fibre Optic Sensing Handbook* (Berlin, Germany: Springer-Verlag, 1990). He has filed 15 patent applications. His current research interests in opto-electronics include all optical self-routing switches that route data-modulated laser beams according to the destination address encoded within the data signal, ultrafast three-wave opto-electronic detectors, mixers and phase-locked loops , and distributed fiber optic sensors. In the RF/microwave area, his interests include the theory and design of low-noise oscillators using inductor capacitor (*LC*), surface acoustic wave (SAW), crystal, dielectric, transmission line, helical, and superconducting resonators, flicker noise measurement and reduction in amplifiers and oscillators, high-efficiency broad-band amplifiers, broad-band negative group-delay circuits, and high-Q printed filters with low radiation loss and monolithic-microwave integrated-circuit (MMIC) implementations.

Dr. Everard is a member of the Institution of Electrical Engineers (IEE), U.K.